What is claimed is:

1. A signal chain for an image sensor, comprising:

a plurality of photo sensing elements;

a plurality of pixel readout circuits, each pixel readout circuit operating to receive a charge-induced signal and a reset signal from a photo sensing element, and to compute a difference signal between said charge-induced signal and said reset signal, said difference signal being measured with respect to a reference signal; and

an amplifier configured to receive said reference signal, and to supply said reference signal to said plurality of pixel readout circuits during computation of said difference signal, where said amplifier amplifies said difference signal when the computation is completed.

2. The signal chain of claim 1, further comprising:

a plurality of A-to-D converters operating to alternately convert said amplified difference signal.

3. The signal chain of claim 2, wherein each of said plurality of A-to-D converters includes a binary-scaled capacitor network capable of sampling and converting said reference signal to a digital value.

4. The signal chain of claim 3, wherein said each of said plurality of A-to-D converters includes a latch to save the converted difference signal.

5. The signal chain of claim 3, wherein said plurality of A-to-D converters includes:

a first A-to-D converter arranged into a first configuration operating to convert said amplified difference signal in a particular cycle; and

a second A-to-D converter arranged into a second configuration operating to sample a next amplified difference signal into said binary scaled capacitor network in said particular cycle,

wherein said first and said second A-to-D converters switch configurations in a cycle after said particular cycle.

6. The signal chain of claim 2, further comprising:

a multiplexer configured to sequentially output saved difference signal in said latch.

7. The signal chain of claim 1, wherein said plurality of photo sensing elements is a pixel array arranged in columns of pixels.

8. The signal chain of claim 1, wherein said each pixel readout circuit includes at least two capacitive elements, one to hold pixel reset value, and another to compute and store said difference signal between said charge-induced signal and said reset signal.

9. The signal chain of claim 1, wherein said amplifier includes a feedback switch operating to provide said reference signal, received at a negative input to said amplifier, to said each pixel readout circuit through a feedback.

10. The signal chain of claim 1, wherein said each pixel readout circuit includes a column select switch to connect selected column pixel readout to said amplifier.

11. The signal chain of claim 10, wherein said column select switch is a p-channel MOSFET (PMOS) transistor.

12. The signal chain of claim 1, wherein said each pixel readout circuit includes a sample and hold switch to sequentially read said charge-induced signal and said reset signal.

13. The signal chain of claim 12, wherein said sample and hold switch is an n-channel MOSFET (NMOS) transistor.

14. The signal chain of claim 1, further comprising:

a sample and hold circuit coupled to said reference signal, said sample and hold circuit operating to provide stable reference signal.

15. The signal chain of claim 14, wherein said signal smoothing circuit includes:

a reference signal generator operating to generate the reference signal;

at least one switch configured to sample and hold the reference signal at a certain level; and

a capacitor coupled to said at least one switch, said capacitor operating to hold the sampled value at the certain level.

16. The signal chain of claim 15, wherein said reference signal generator includes a voltage divider resistor network.

17. The signal chain of claim 15, wherein said at least one switch includes MOSFET transistors.

18. An image sensor output circuit, comprising:

a pixel array having a series of pixels, and operating to receive optical data and convert said optical data into electrical signals;

readout circuits configured to read said electrical signals from said series of pixels with respect to a reference signal;

an amplifier configured to provide said reference signal while said readout circuit is reading said electrical signal, and to provide amplification of said referenced electrical signals when the reading is done; and

at least one A-to-D converter operating to provide conversion of said amplified electrical signal.

19. The circuit of claim 18, wherein said at least one A-to-D converter includes first and second A-to-D converters, said first A-to-D converter converting said reference electrical signal while said second A-to-D converter is sampling a next reference electrical signal.

20. The circuit of claim 18, further comprising:

a multiplexer configured to sequentially output converted signals.

21. An image senor comprising:

a pixel array having a plurality of pixels;

a plurality of pixel readout circuits, each pixel readout circuit operating to receive a charge-induced signal and a reset signal from a pixel of said pixel array, and to compute a difference signal between said charge-induced signal and said reset signal, said difference signal being measured with respect to a reference signal;

an amplifier coupled to said each pixel readout circuit, said amplifier configured to supply said reference signal during computation of said difference signal, and to amplify said difference signal when the computation is done;

a pixel array addressing circuit configured to select a group of pixels in said pixel array to readout; and

a controller coupled to said pixel array addressing circuit, and operating to provide selection control to said pixel array addressing circuit.